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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,913	06/20/2001	Jeffrey Lukanc	IDT-1616	7471

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EXAMINER	
YUFA, ALEKSANDR L	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 10/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,913	LUKANC, JEFFREY	
	Examiner	Art Unit	
	Alex Yufa, Ph.D.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because the subject matter "An integrated circuit chip" is not descriptive for "Test bus architecture for ...".

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant claims the "integrated circuit chip" disclosing the "test bus architecture for ..." (see title of the invention). Also, the term " integrated circuit chip " in claims 1-10 is a term which renders the claim indefinite. The term " integrated circuit chip " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably appraised of the scope of the invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph.

Claim 4 recites the limitation "a plurality of RAM blocks". There is insufficient antecedent basis for this limitation in the claim 2.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

A. Determining the scope and contents of the prior art.
B. Ascertaining the differences between the prior art and the claims at issue.
C. Resolving the level of ordinary skill in the pertinent art.
D. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,568,437 to Jamal.

Referring to claim 1, Jamal discloses the built-in-self-test for integrated circuits having read/write memory. Jamal teaches to use "an integrated circuit 80" with random access memory (RAM)" 84 (see e.g. abstract, line 1 and Fig. 2a), "the built-in self tester

(test module) 100" for the RAM (see e.g. abstract, line 2 and Fig. 2a), and "a bus" (see "the RAM BIST controller 102 /see Fig. 4/ generates test data for the RAM 84 and transmits it over the data bus ... /see column 5, lines 11, 12/). Jamal does not explicitly point out to multiplication (integration) of the elements, but Jamal does not limit such well known feature, inherently teaching for using of any degree of element integration inside the chip, that is well known in the integrated circuits (IC) industry.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal technique by providing multi-identical-element chip, because one of ordinary skill in the art would use well known and obvious plurality principles to create an integration of well known elements into one chip considering also well known and obvious integrated circuit industry practice.

Claims 2-10 depend from respective claim 1, hence inherit the rejection in claim 1. Also, according claims 2, 3, Jamal teaches to use pads (see, for example, "in this technique, multiplexers provide paths from IC input/output (I/O) pads to the targeted subcircuit" /column 1, lines 18-20/), and "an integrated circuit, wherein the RAM BIST controller comprises switching logic which, in response to signals, decouples said BIST and said RAM from other components on the integrated circuit and couples said BIST RAM controller to the RAM" (column 10, lines 45-50).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use and/or modify Jamal switching means, because one of ordinary skill in the art would use well known Jamal's

switching principles in order to provide the coupling, for example, the test bus and the circuitry.

Referring to claim 4, Jamal discloses the built-in self tester (BIST), which "is coupled to the RAM and to input/output (I/O) ports" (column 2, lines 51, 52), "within the industry, TAP denotes the IEEE 1149.1 input/output test convention. The standard dictates four pins: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). An optional test reset (TRST) pin is also provided by the TAP standard." (column 2, lines 7-11).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use and/or modify Jamal ports, because one of ordinary skill in the art would use well known Jamal's ports and standard requirements in order to provide RAM (and/or other means).

Referring to claim 5, Jamal teaches that "the RAM BIST controller 102 generates test data for the RAM 84 and transmits it over the data bus of width W_D. The controller 102 also transmits control signals to the RAM over control line of width W_C to addresses within the RAM. The addresses are specified by the RAM BIST controller 102 and transmitted to the RAM 84 over the address line of W_A" (column 5, lines 11-15), and "a latch enable signal commands a BIST register to latch the address of the malfunctioning location in the RAM 84" (column 4, lines 29, 30).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's standard lines or modify them, because one of ordinary skill in the art would use well known

address/data/control signal interchange technique in order to provide signal communication between means.

According claim 6, Jamal discloses that the "generated test enable signals switch the multiplexers into test mode (column 1, lines 20, 21). Upon receipt of the scan mode enable signal, the BIST can receive initialization data through a "scan in" line, or the BIST (column 4, lines 4-6).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's line or modify it, because one of ordinary skill in the art would use transmitting line for transmission of well known enable signals to the test modules, considering well known and obvious use of the enable signal transmitting technique.

Referring to claim 7, Jamal discloses that the "the RAM BIST controller controls the RAM during a test where the RAM includes data, address, and control lines" (column 2, lines 54-56).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's line or modify it, because one of ordinary skill in the art would use transmitting line for transmission of well known data value, considering well known and obvious use of the data transmitting technique.

According claim 8, Jamal discloses "unique address", data storage" (column 2, line 31), and that the "data storage locations, and each location has a unique address" (column 2, lines 30, 31), and "the input/output circuitry includes a register capable of

storing address, data, and control signal information of a read/write memory ..." (column 2, lines 40-43). Also Jamal teaches that "the BIST I/O is ... capable of storing an address of a data storage location in the RAM ..." (column 2, lines 60-62), and "A test mode or test enable signal is received by a RAM BIST controller 102 initializes registers within the RAM BIST controller 102 ..." (column 5, lines 3-5).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal's data storages and "unique address", because one of ordinary skill in the art would simply use or modify well known and obvious address storing technique in order to provide storing of "unique address".

Referring to claim 9, Jamal discloses that the "multiplexer or "functional block" isolation is one approach to testing these subcircuits. In this technique, multiplexers provide paths from IC input/output (I/O) pads to the targeted subcircuit"(column 1, lines 17-20), and "functional block isolation suffer from several disadvantages, however, including multiplexer delays, routing congestion, and the need for externally generated test vectors or signals" (column 1, lines 21-24).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Jamal's multiplexing principles and multiplexers or modify them, because one of ordinary skill in the art would use well known multiplexers for routing signals from the corresponding blocks, considering well known and obvious multiplexing technique.

Claims 2-9 are rejected as depended from respective claim 1, hence inherit the deficiency in claim 1.

8. Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,568,437 to Jamal in view of US 5,515,540 to Grider et al.

Referring to claim 10, Jamal discloses RAM and does not explicitly point out and limit RAM capacity, inherently teaching for using of any reasonably applicable kinds of RAMs and their capacities, but Grider et al. teaches that "the embedded address and data busses are used on the DS5000FP to connect to external byte-wide memory devices. Pins A0-A14 address up to 32 KBytes of Program/Data memory which is transferred over pins ED0-ED7 (a bidirectional port). An additional 32 Kbytes of data memory (cannot be used for program memory) can be addressed by using ECE2* (manipulation of ECE2* is described in the DS5000 data sheet)" (column 6, lines 50-57).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Jamal with the teaching of Girder et al. by simply using RAM with the limited capacity, because one of ordinary skill in the art would easier use the smaller RAM's capacity in order to achieve higher reliability.

According claim 11, Jamal discloses that "during normal mode, the RAM 84 may be connected to other system signals through the BIST 100. In other words, BIST circuitry 100 interfaces the RAM 84 to other components on the integrated circuit ..." (column 6, lines 59-62), and "the RAM BIST controller controls the RAM during a test

[test mode] where the RAM includes data, address, and control lines Jamal, disclosing RAM, does not explicitly point out and limit RAM capacity, inherently teaching for using of any reasonably applicable kinds of RAMs and their capacities, but Grider et al. teaches that "the embedded address and data busses are used on the DS5000FP to connect to external byte-wide memory devices. Pins A0-A14 address up to 32 KBytes of Program/Data memory which is transferred over pins ED0-ED7 (a bidirectional port). An additional 32 Kbytes of data memory (cannot be used for program memory) can be addressed by using ECE2* (manipulation of ECE2* is described in the DS5000 data sheet)" (column 6, lines 50-57).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Jamal with the teaching of Girder et al. by simply using normal and test modes for 32 Kbytes RAM operation, because one of ordinary skill in the art would easier use well known and obvious access to the RAM in normal functional regime and in the test regime in order to provide the normal operation and testing of the random access memory.

Referring to claim 12, Jamal discloses that "the controller 102 also transmits control signals to the RAM over control line of width W_C ..." (column 5, lines 12-14). Also, Grider et al. teaches that "memory ... include the ability to address 128K bytes of NV SRAM on the bytewide bus, multiple memory architectures for optimum implementation, and a peripheral memory map" (column 8, lines 47-50).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal with the teaching of

Girder et al. by simply using test control line (bus), because one of ordinary skill in the art would use the test control line (bus) during the test regime (mode) in order to provide testing operation of the memory.

Referring to claims 13, 14, the examiner interprets claims 13 and 14 as being similar to claims 8 and 2 respectively, therefore claims 13 and 14 are rejected based on the same rationale thereof.

Referring claim 15, Jamal teaches that the "BIST controller" controls the pad switching (column 10, line 45). Jamal does not call his "BIST controller" as JTAG, but provides "BIST controller" with the analogous functions.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal's BIST controller, because one of ordinary skill in the art would use the any type controller, providing analogous controlling functions for coupling of the pads in order to switch system circuitry during normal or test modes.

According claims 16, 17, Jamal describes "an integrated circuit with read/write memory and an improved read/write memory self testing capability" (column 2, lines 26-28), and teaches that "the method includes activating a read/write memory location on the integrated circuit and activating a built-in self tester (BIST) on the integrated circuit. The BIST writes test data to the memory location and reads the test data as retrieved data from the same memory location' (column 2, lines 66, 67 and column 3, lines 1-3). Also, Grider teaches to use "Embedded Bus Read/Write" (column 6, line 44).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal with the teaching of Girder et al. by simply using test bus, because one of ordinary skill in the art would use the test control line (bus) during the test regime (mode) in order to provide writing/reading operation of the RAM blocks.

According claim 18, Jamal teaches that "the test clock signal clocks the BIST circuitry 12 and testing operations performed by the BIST on the RAM 14 (column 1, lines46-48), and "a "scan clock" line produces a clocking signal for the scan in or shift in operation" (column 4, lines 7, 8).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Jamal's "clocking signal", because one of ordinary skill in the art would use well known timing principles, considering well known and obvious methods for bus operating in response to clock signal during the selected mode.

Conclusion

9. The following are suggested formats for either a Certificate of Mailing or Certificate of Transmission under 37 CFR 1.8(a). The certification may be included with all correspondence concerning this application or proceeding to establish a date of mailing or transmission under 37 CFR 1.8(a). Proper use of this procedure will result in such communication being considered as timely if the established date is within the required period for reply. The Certificate should be signed by the individual actually

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Please refer to 37 CFR 1.6(d) and 1.8(a)(2) for filing limitations concerning facsimile transmissions and mailing, respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex Yufa whose telephone number is 703-305-0715. The examiner can normally be reached on M-F 8:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2394.

Alex Yufa, Ph.D.
Examiner
Art Unit 2133

aly

Gregory J. Lamaire
for
Albert DeCady
Primary Examiner